Amendments to the Specification

1. Please amend lines 19-24 at page 9 with the following amended paragraph:

The circuit of FIG 7 recovers the ~~network link clock RN~~ master clock signal RT through the following process: After an initial acquisition period, the timing loop will reach a steady state where the output clock frequency RR matches the transmitter frequency FT. Then the modulus circuitry comprising of 250, 252, 260, and 262 will re-create the phase variations of RN around the reconstructed clock RT by way of repeating the process followed at the transmitter (FIG. 5).